In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) An integrated circuit, comprising:

a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array;

a programmable non-volatile configuration memory, adapted to store the configuration data;

memory storing instructions for a mission function for the integrated circuit, [[and]] storing instructions for a configuration function used to transfer the configuration data from the programmable non-volatile configuration memory to the programmable configuration points within the configurable logic array;

memory protected from overwriting or modification by an in circuit programming function and storing instructions for a configuration load backup function used to recover from an incomplete transfer of the configuration data from the programmable non-volatile configuration memory to the programmable configuration points within the configurable logic array; and

a processor coupled to the memory which fetches and executes said instructions from the memory.

2. (original) The integrated circuit of claim 1, wherein said memory comprises a non-volatile store.

3. (original) The integrated circuit of claim 1, wherein said memory comprises a floating gate memory store.

4. (original) The integrated circuit of claim 1, wherein said memory comprises a read-only memory store.

5. (original) The integrated circuit of claim 1, wherein said memory comprises a first non-volatile store for the configuration function, and a second store for the mission function.

6. (original) The integrated circuit of claim 1, wherein said memory comprises a first volatile store for the configuration function, and a second store for the mission function.

7. (original) The integrated circuit of claim 1, including a watchdog timer coupled to the processor, and wherein the configuration function includes using the watchdog timer.

8. (previously presented) The integrated circuit of claim 1, wherein the configuration function includes loading the programmable non-volatile configuration memory via an input port on the integrated circuit.

9. (previously presented) The integrated circuit of claim 1, wherein the configuration function includes receiving encrypted configuration data via an input port on the integrated circuit, decrypting the configuration data, and loading the programmable non-volatile configuration memory with decrypted configuration data.

10. (previously presented) The integrated circuit of claim 1, wherein the configuration function includes receiving compressed configuration data via an input port on the integrated circuit, decompressing the configuration data, and loading the programmable non-volatile configuration memory with decompressed configuration data.

11-12. (canceled).

13. (original) The integrated circuit of claim 1, wherein the electrically programmable configuration points comprise non-volatile, charge programmable memory cells.

14. (previously presented) The integrated circuit of claim 1, wherein the configuration function includes loading the programmable non-volatile configuration memory via an input port on the integrated circuit, and including:

an interface between the processor and the programmable non-volatile configuration memory supporting said loading; and

an interface between the programmable non-volatile configuration memory and the configurable logic array supporting said transfer of configuration data to the configurable logic array.

15. (previously presented) The integrated circuit of claim 1, wherein the configuration function includes loading the programmable non-volatile configuration memory via an input port on the integrated circuit, and including:

an interface between the processor and the programmable non-volatile configuration memory supporting said loading and said transfer of configuration data to the configurable logic array; and

an interface between the processor and the configurable logic array supporting said transfer of configuration data to the configurable logic array.

16. (previously renumbered as 15).

17. (canceled).

18. (previously presented) The integrated circuit of claim 1, wherein the interface between the programmable non-volatile configuration memory and the configuration logic array comprises a dedicated data path for said transfer of configuration data to the programmable logic array.

19. (previously presented) The integrated circuit of claim 1, wherein the interface between the programmable non-volatile configuration memory and the configuration logic array comprises a data path including the processor for said transfer of configuration data to the programmable logic array.

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